

# ● PRINTER RUSH ●

## (PTO ASSISTANCE)

Application : <u>09/747,188</u>	Examiner : <u>Bayard</u>	GAU : <u>2631</u>
From : <u>PAP</u>	Location : <u>IDO</u> FMF FDC	Date : <u>7/29/05</u>

Tracking #: EPM 09/747,188 Week Date: 5/16/05

DOC CODE	DOC DATE	MISCELLANEOUS
<input type="checkbox"/> 1449	_____	<input type="checkbox"/> Continuing Data
<input type="checkbox"/> IDS	_____	<input type="checkbox"/> Foreign Priority
<input type="checkbox"/> CLM	_____	<input type="checkbox"/> Document Legibility
<input type="checkbox"/> IIFW	_____	<input type="checkbox"/> Fees
<input type="checkbox"/> SRFW	_____	<input type="checkbox"/> Other
<input type="checkbox"/> DRW	_____	
<input type="checkbox"/> OATH	_____	
<input type="checkbox"/> 312	_____	
<input checked="" type="checkbox"/> SPEC	<u>3/19/01</u>	

[RUSH] MESSAGE: please verify serial No. for  
Attorney Docket No. 0325.00388 found on page 1, lines  
11 and 12 of SPEC of 3/19/01.

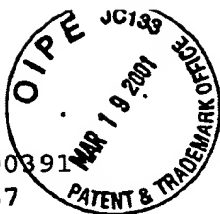
Thank you.

[XRUSH] RESPONSE: See attached with serial numbers.

INITIALS: MS

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.

0325.00391  
CD00087



09/747,188

LINEARIZED DIGITAL PHASE-LOCKED LOOP METHOD

TECHNOLOGY CENTER 2600

This application claims the benefit of U.S. Provisional  
Application No. 60/203,610, filed May 12, 2000 and is hereby  
5 incorporated by reference in its entirety.

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Cross Reference to Related Applications

Technology Center 2600

The present application may relate to co-pending  
application Serial No. 09/745660, (Attorney Docket No. 0325.00386)  
10 filed December 21, 2000, Serial No. 09/747281, (Attorney Docket  
No. 0325.00387) filed December 21, 2000, Serial No. 60/203677,  
(Attorney Docket No. 0325.00388) filed December 22, 2000, Serial  
No. 09/747262, (Attorney Docket No. 0325.00389) filed December 22,  
2000, and Serial No. 09/746802, (Attorney Docket No. 0325.00390)  
15 filed December 22, 2000, which are each hereby incorporated by  
reference in their entirety.

Field of the Invention

The present invention relates to a method and/or  
20 architecture for implementing phase-locked loops (PLLs) generally